



LNA for Agilent flow demonstration

Reuven Holzer

Oct/20/2010

The Global Specialty Foundry Leader

Agenda

- Back-Ground
- Specifications
- Development scheme
- 3 Currents amplifier
- Final Amplifier
- 1 Tone simulation
- 2 tones simulation
- Layout
- Layout for momentum
- Post layout with pre layout values
- Post Layout with adjusted values
- Summary

Back-Ground

- In this work we prepare an LNA design
 - Prove Agilent flow with TowerJazz ASD PDK
- In order to meet short schedule
 - Implement simple single ended LNA matched to 50Ω both output and input
 - Do design without package consideration (Assume on chip source and loads).
 - Not Fully optimize transistor sizes and operating points
 - Did “out of the Characterization Document” OP
 - Did not match input for lowest NF
- In This document we describe only simulations in Typical conditions
- TBD:
 - Layout
 - Momentum
 - Comparison Pre/Post Layout results

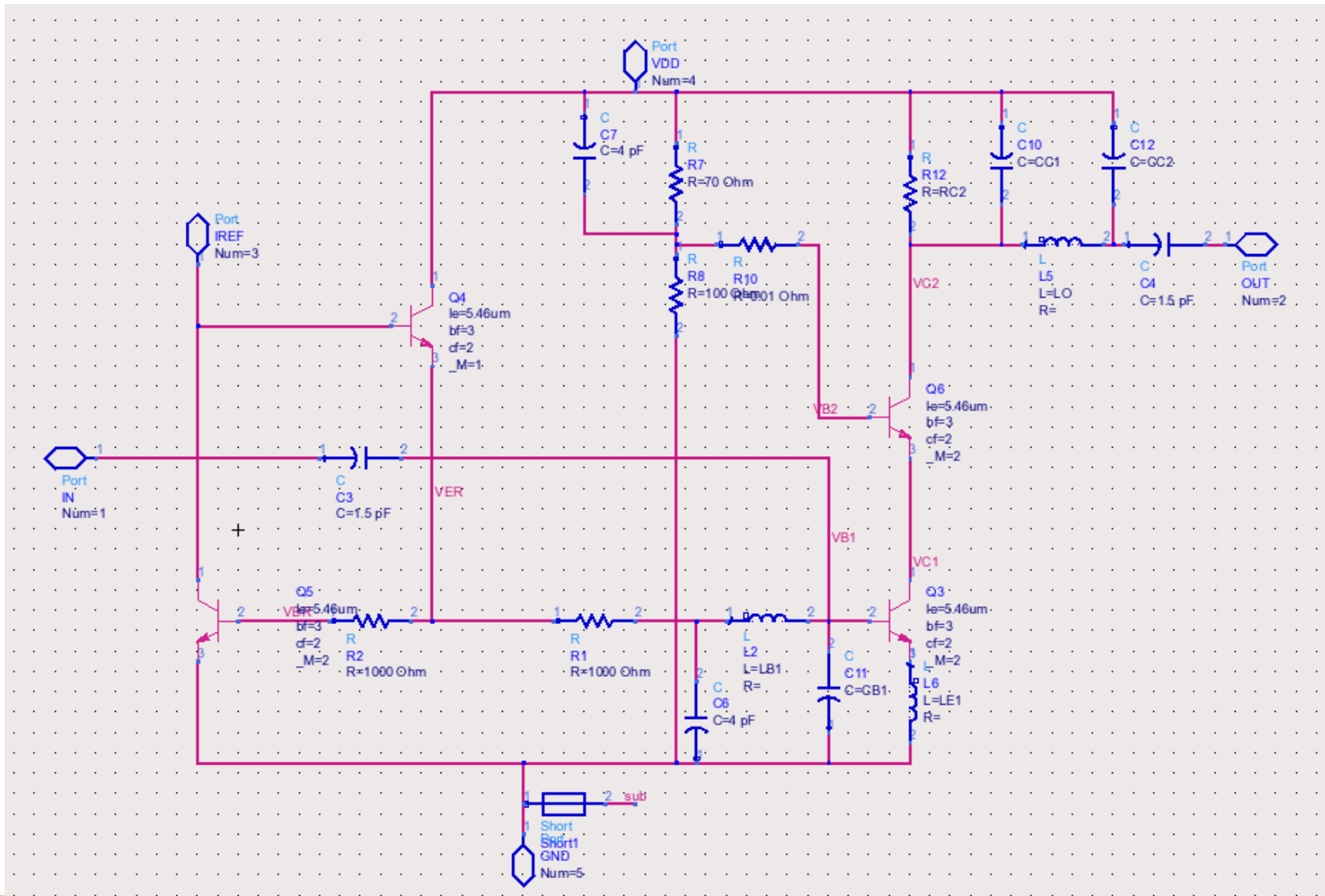
Specifications – Typical (De Facto)

Parameter	Unit	Typical	Min	Max
VDD	Volt	3.3	3	3.6
Temp	°C	27	-40	120
Center frequency	GHz	24	23.5	24.5
BW	GHz	3	2	4
Input Impedance	Ω	50	35	65
Output Impedance	Ω	50	35	55
Power Gain	dB	13	12	15
NF	dB	5	4.5	5.5
1 dB compression (input)	dBm	-15	-16	-17
IIP3	dBm	-6	-7	-5

Simulations In Typical Conditions

- Typical Corner, VDD = 3.3V, TEMP = 27°C

LNA – Lumped components schematics



2.5mA,

Var
Eqn

VAR
VAR1
IDC=2.5e-3
ZIN=50
ZOUT=50
LB1=2.2e-10
LE1=1e-12
LC2=1e-6
RC2=400
CC1=1.5e-14
CC2=1e-15
LO=7e-10
CB1=1e-15

5mA,

Var
Eqn

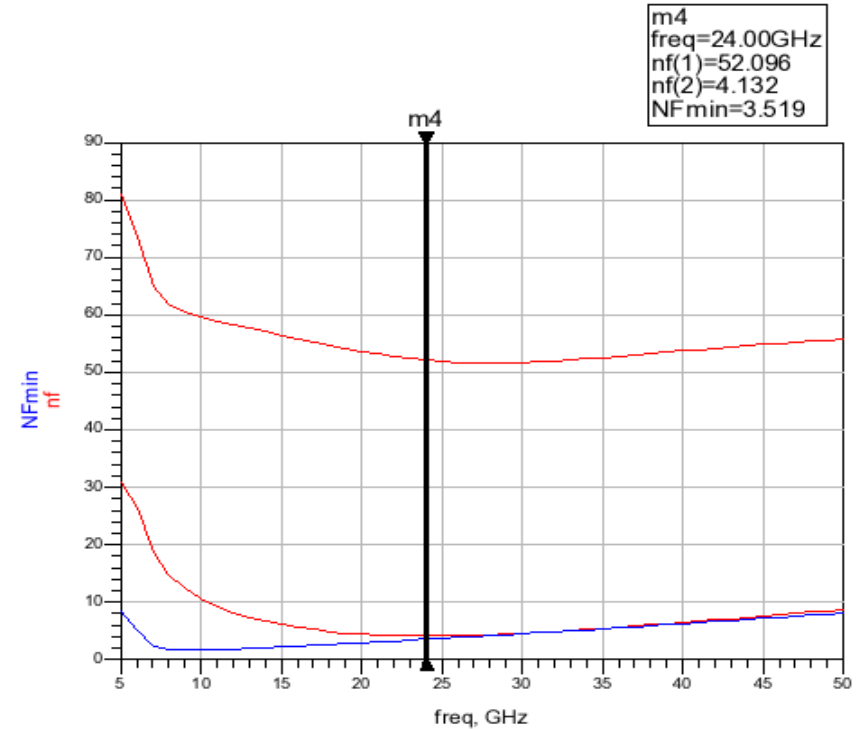
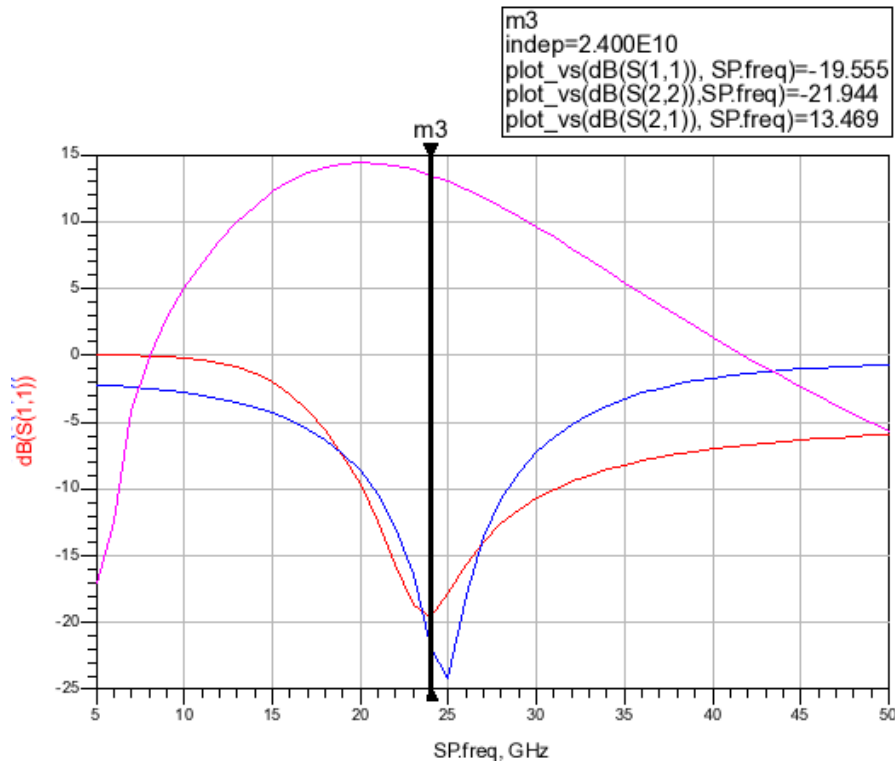
VAR
VAR1
IDC=5e-3
ZIN=50
ZOUT=50
LB1=1.8e-10
LE1=1e-12
LC2=1e-6
RC2=200
CC1=3e-14
CC2=1e-15
LO=5e-10
CB1=1e-15

10mA

Var
Eqn

VAR
VAR1
IDC=1e-2
ZIN=50
ZOUT=50
LB1=5e-10
LE1=1e-10
LC2=1e-6
RC2=100
CC1=3e-14
CC2=1e-15
LO=3e-10
CB1=6e-14

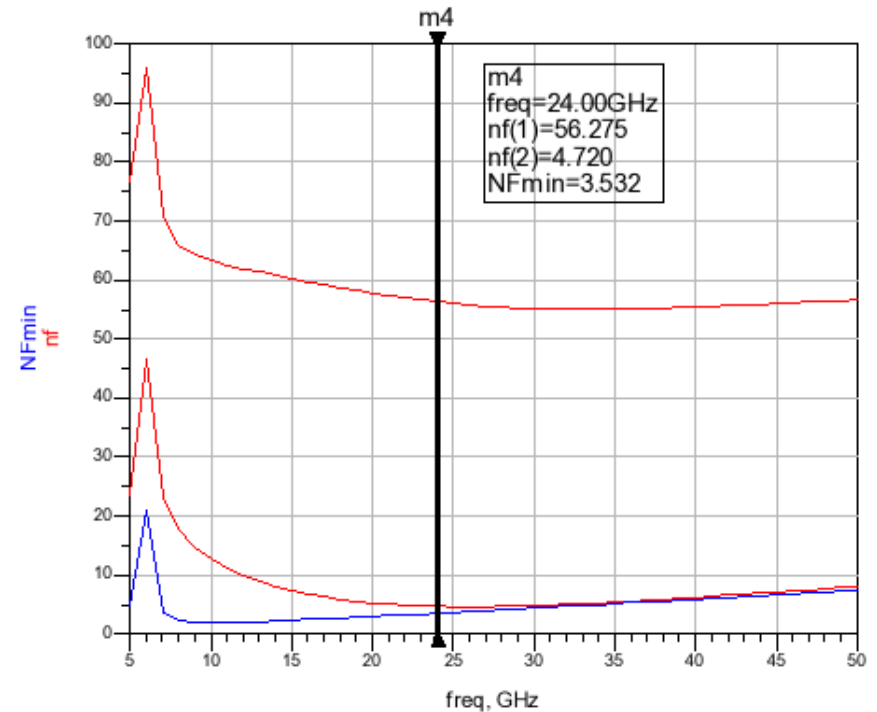
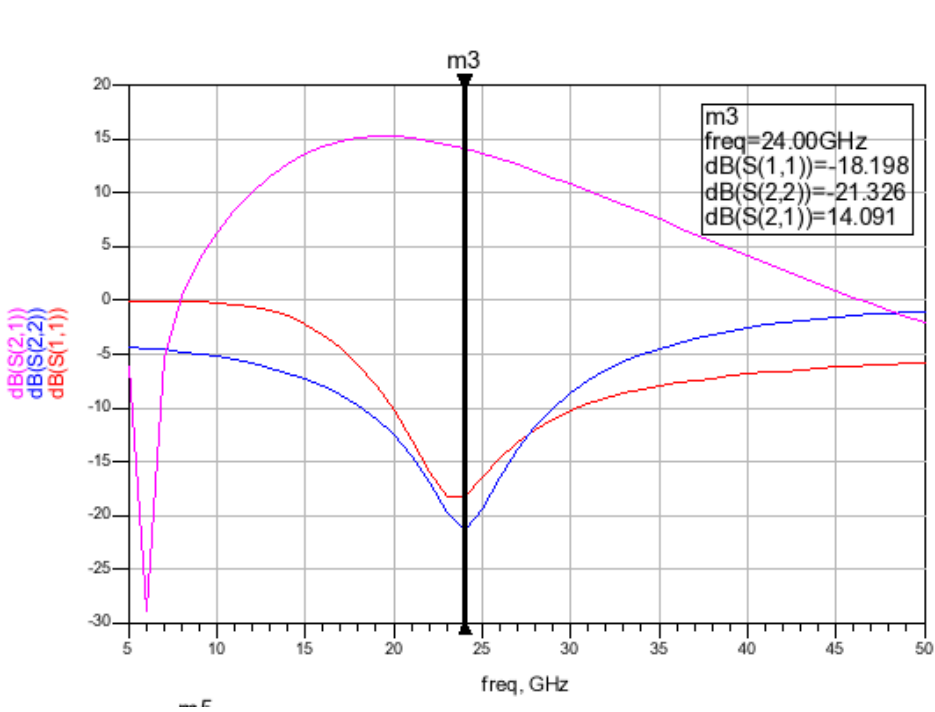
DC and SP for 2.5mA LNA



freq	VB1	VC1	VB2	VC2
0.0000 Hz	846.8 mV	1.094 V	1.940 V	2.320 V

freq	...q.P1.pinCurrent.i	...q.P2.pinCurrent.i	...q.P3.pinCurrent.i	Q6.P1.pinCurrent.i	Q6.P2.pinCurrent.i	Q6.P3.pinCurrent.i
0.0000 Hz	2.470 mA	19.49 uA	-2.490 mA	2.451 mA	19.27 uA	-2.470 mA

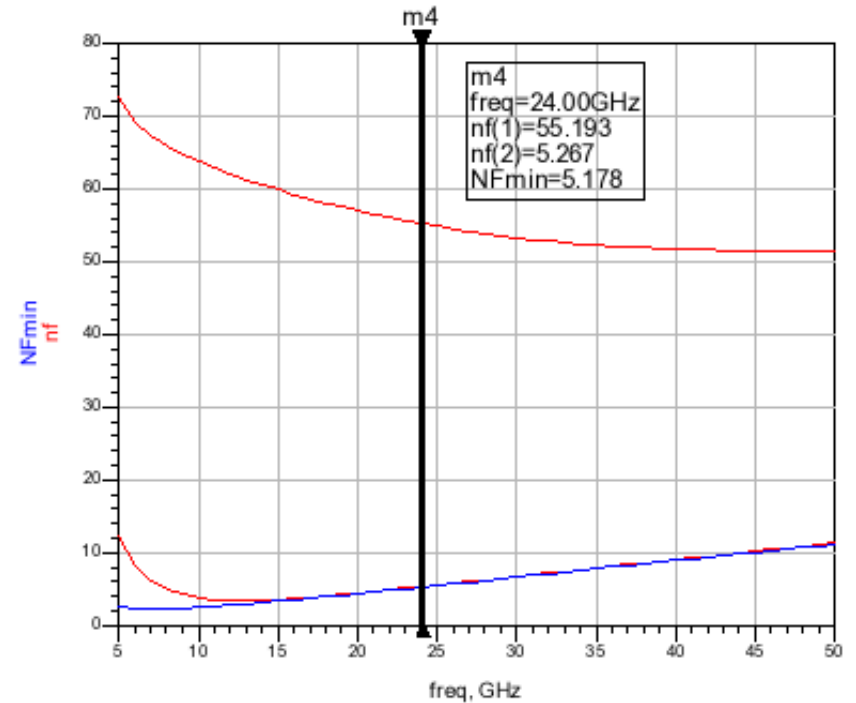
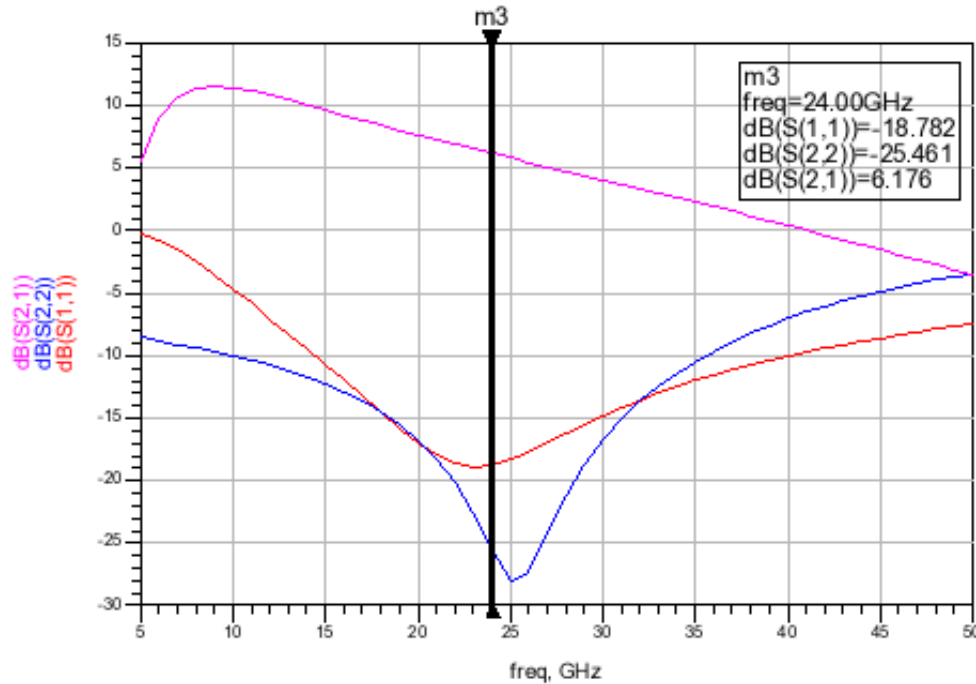
DC and SP for 5mA LNA



freq	VB1	VC1	VB2	VC2
0.0000 Hz	867.7 mV	1.072 V	1.940 V	2.319 V

freq	...q.P1.pinCurrent.i	...q.P2.pinCurrent.i	...q.P3.pinCurrent.i	Q6.P1.pinCurrent.i	Q6.P2.pinCurrent.i	Q6.P3.pinCurrent.i
0.0000 Hz	4.946 mA	40.72 uA	-4.987 mA	4.906 mA	40.22 uA	-4.946 mA

DC and SP for 10mA LNA



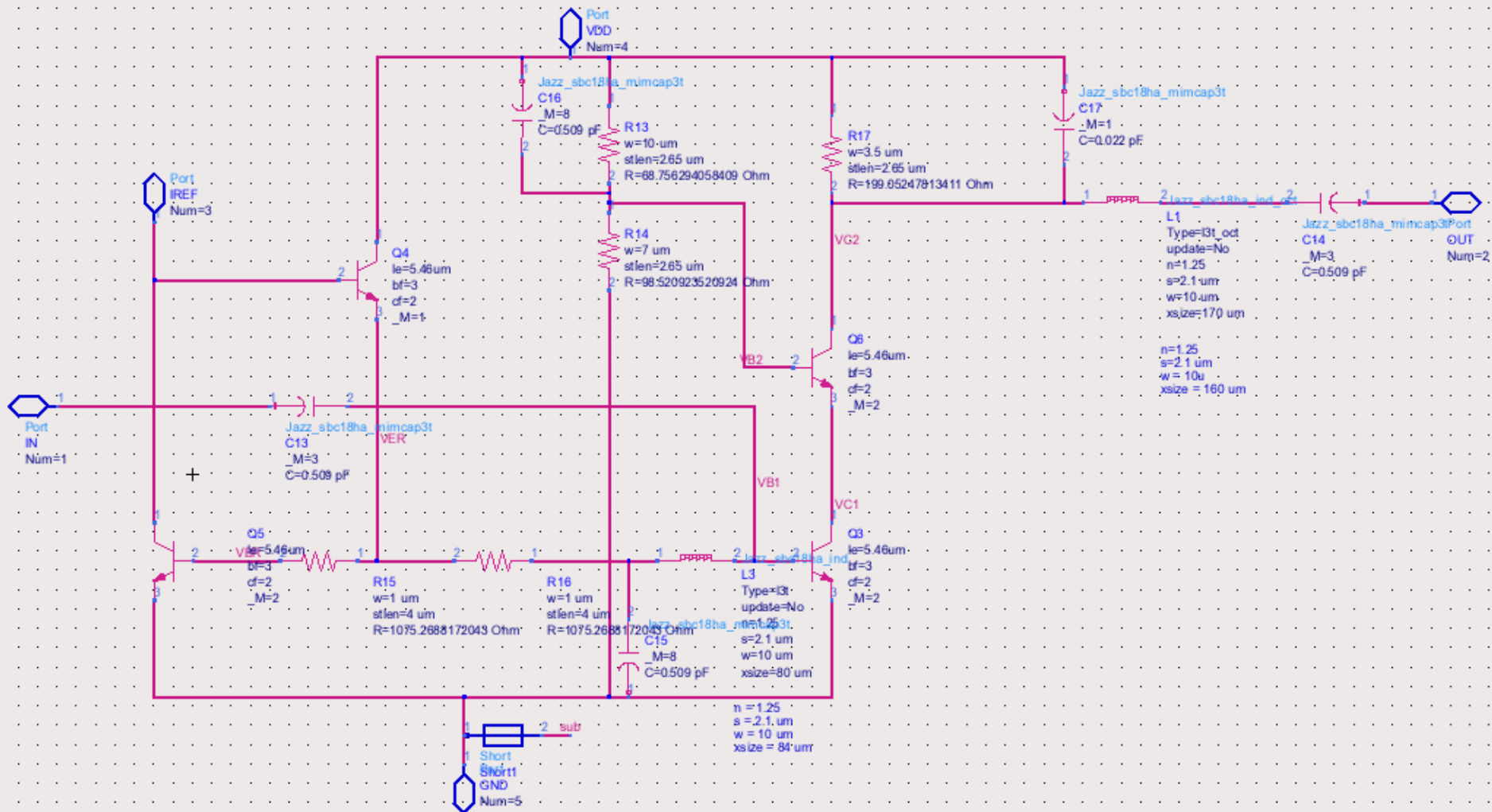
freq	VB1	VC1	VB2	VC2
0.0000 Hz	891.4 mV	1.047 V	1.938 V	2.317 V

freq	...q.P1.pinCurrent.i	...q.P2.pinCurrent.i	...q.P3.pinCurrent.i	Q6.P1.pinCurrent.i	Q6.P2.pinCurrent.i	Q6.P3.pinCurrent.i
0.0000 Hz	9.912 mA	87.37 uA	-9.999 mA	9.825 mA	86.18 uA	-9.912 mA

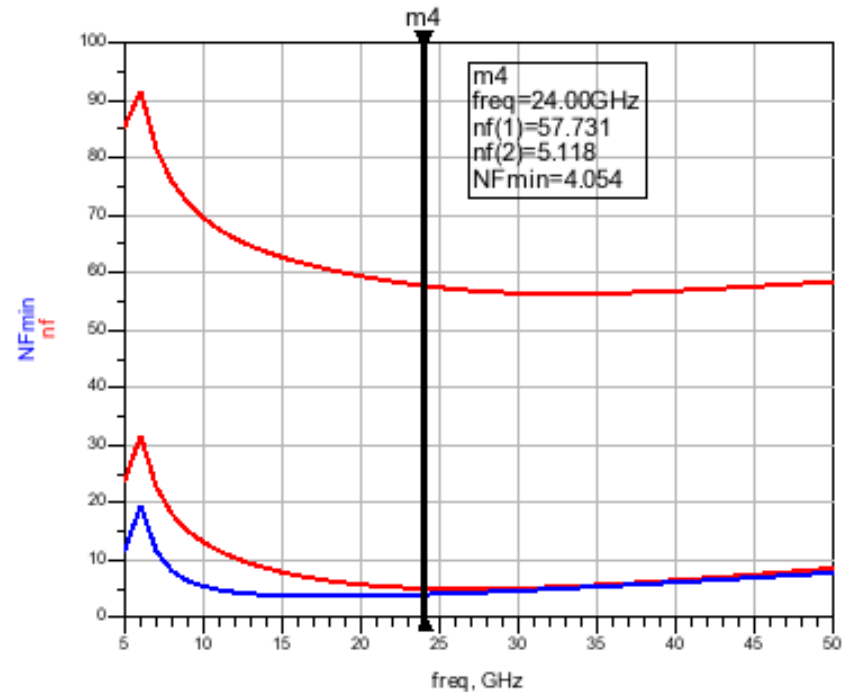
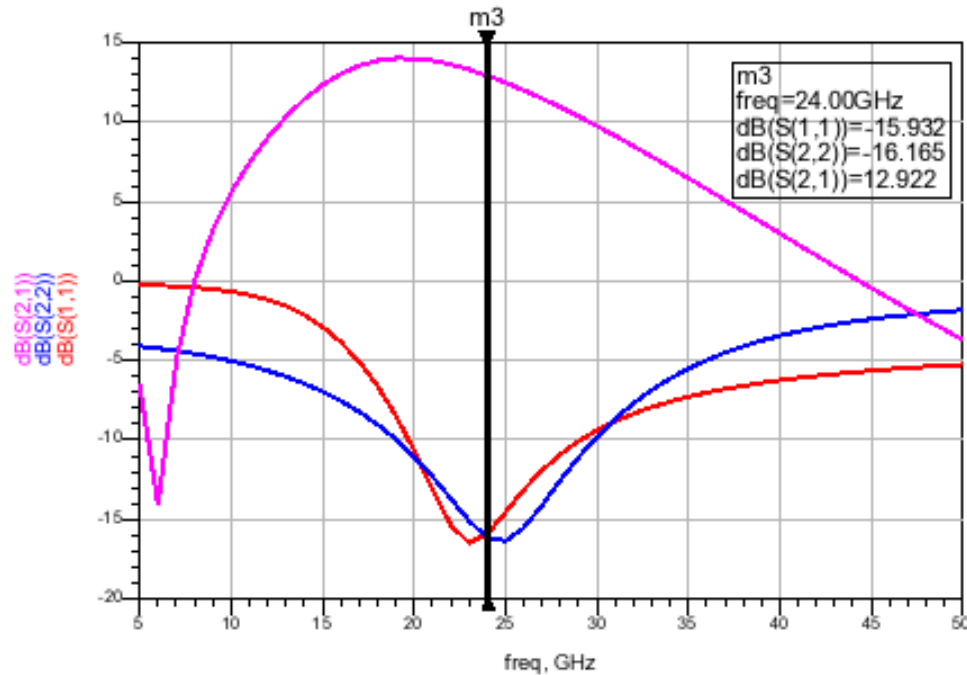
Current decision

- Lowers N_{fmin} at 5mA
- Degradation at 10mA
 - **5mA is considered as max ft OP**
- Designed full PDK version for 5mA LNA

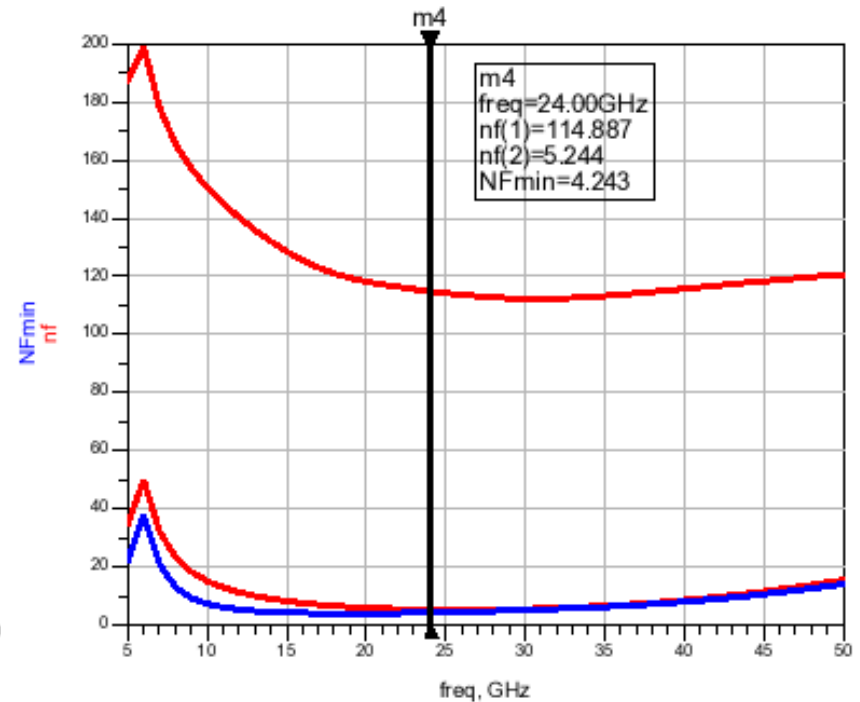
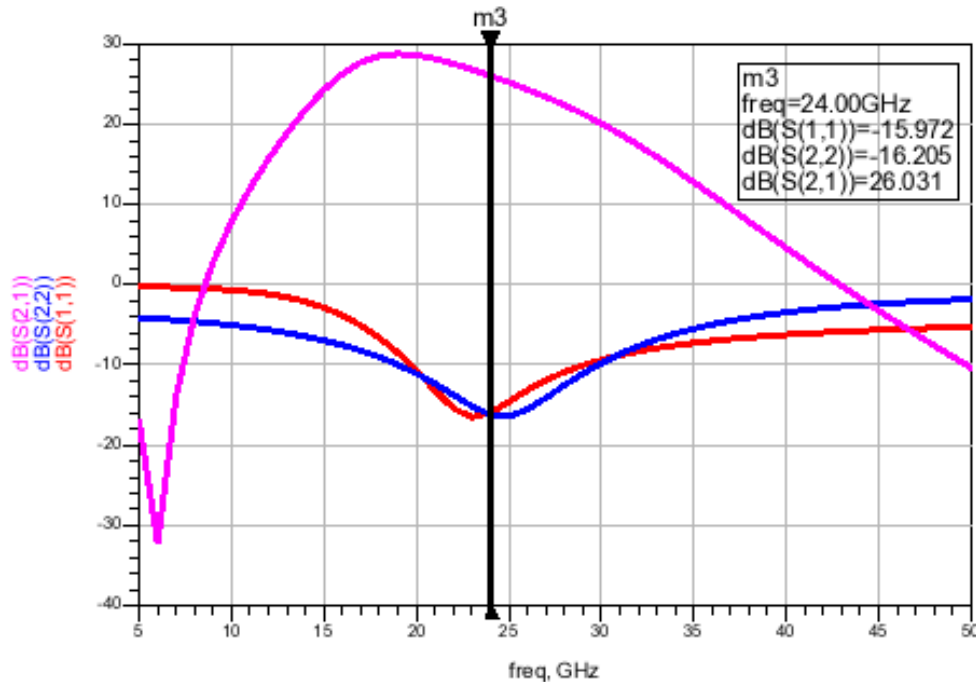
5mA LNA with full Pcell components



DC and SP for LNA with full PDK components

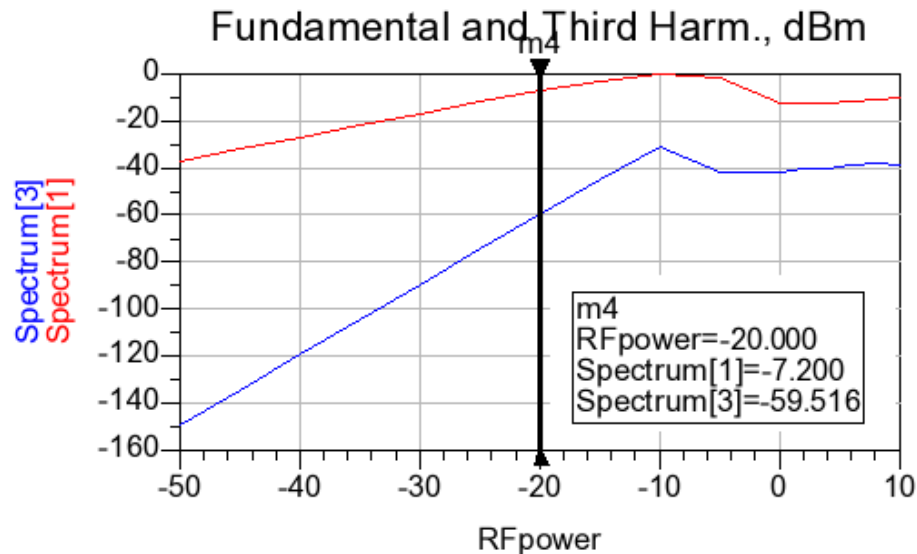


5mA LNA – two cascoded stages



LNA with full PDK components – 1 tone

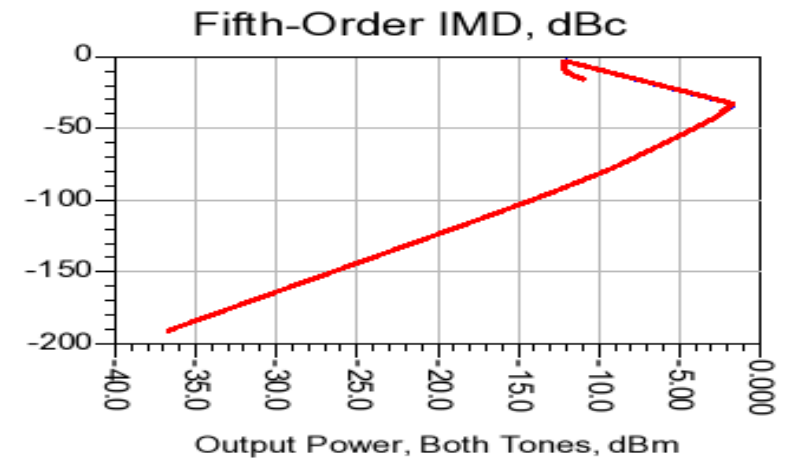
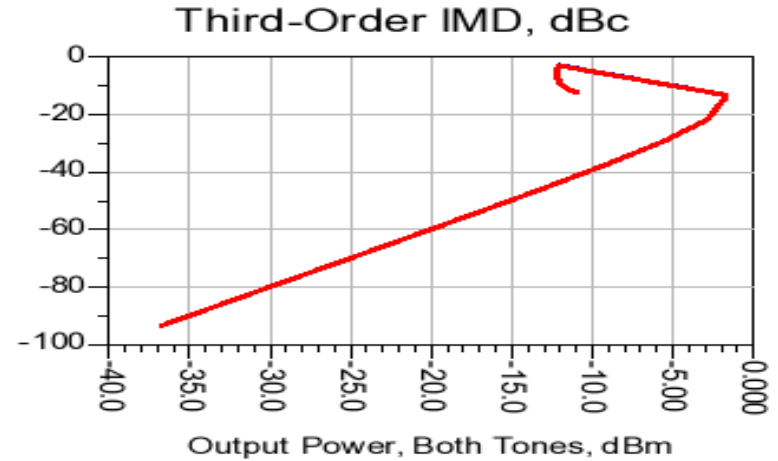
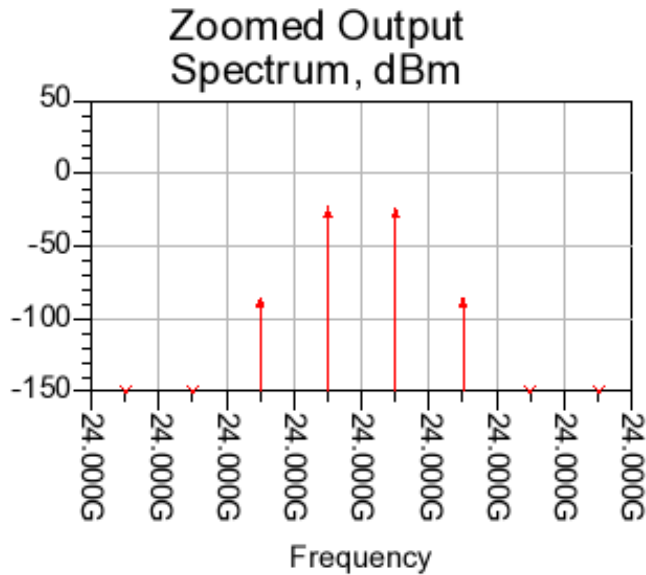
Available Source Power dBm	Fundamental Output Power dBm	Transducer Power Gain	Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
-50.00	-36.84	13.16	-60.23	-112.6	-168.2	-224.7
-45.00	-31.84	13.16	-55.22	-102.6	-153.1	-204.8
-40.00	-26.84	13.16	-50.22	-92.58	-138.1	-184.8
-35.00	-21.85	13.15	-45.22	-82.58	-123.1	-164.7
-30.00	-16.87	13.13	-40.20	-72.55	-107.9	-144.7
-25.00	-11.95	13.05	-35.15	-62.48	-92.52	-124.5
-20.00	-7.200	12.80	-30.04	-52.32	-76.32	-104.4
-15.00	-2.979	12.02	-25.42	-41.88	-59.18	-82.90
-10.00	-211.2 m	9.789	-31.07	-31.10	-53.28	-58.18
-5.000	-1.385	3.615	-16.48	-40.27	-38.64	-55.60
0.0000	-12.14	-12.14	-25.09	-29.48	-49.98	-52.61



LNA with full PDK components – 2 tones

Available Source Power, Both Tones, dBm	Fundamental Output Power, Both Tones, dBm	Transducer Power Gain	Gain Compression dB	Low and High Side Output TOI Points, dBm		Low and High Side Input TOI Points, dBm	
-50.00	-36.83	13.17	0.0000	6.961	6.961	-6.213	-6.213
-46.00	-32.83	13.17	-818.6 u	6.960	6.960	-6.214	-6.213
-42.00	-28.83	13.17	-2.875 m	6.957	6.957	-6.215	-6.214
-38.00	-24.83	13.17	-8.043 m	6.949	6.950	-6.217	-6.216
-34.00	-20.85	13.15	-21.04 m	6.931	6.932	-6.222	-6.222
-30.00	-16.88	13.12	-53.74 m	6.886	6.886	-6.235	-6.234
-26.00	-12.96	13.04	-136.3 m	6.776	6.776	-6.262	-6.262
-22.00	-9.171	12.83	-344.8 m	6.526	6.527	-6.303	-6.302
-18.00	-5.686	12.31	-860.1 m	6.049	6.049	-6.266	-6.265
-14.00	-2.876	11.12	-2.050	5.000	5.001	-6.124	-6.123
-10.00	-1.640	8.360	-4.814	1.965	2.001	-6.394	-6.358
2.000	-12.11	-14.11	-27.28	-13.72	-13.67	0.392	0.439
4.000	-12.23	-16.23	-29.41	-11.99	-11.93	4.245	4.301
6.000	-11.95	-17.95	-31.13	-10.22	-10.28	7.735	7.675
8.000	-11.53	-19.53	-32.71	-8.921	-9.038	10.613	10.496
10.00	-11.02	-21.02	-34.19	-7.916	-7.958	13.102	13.060

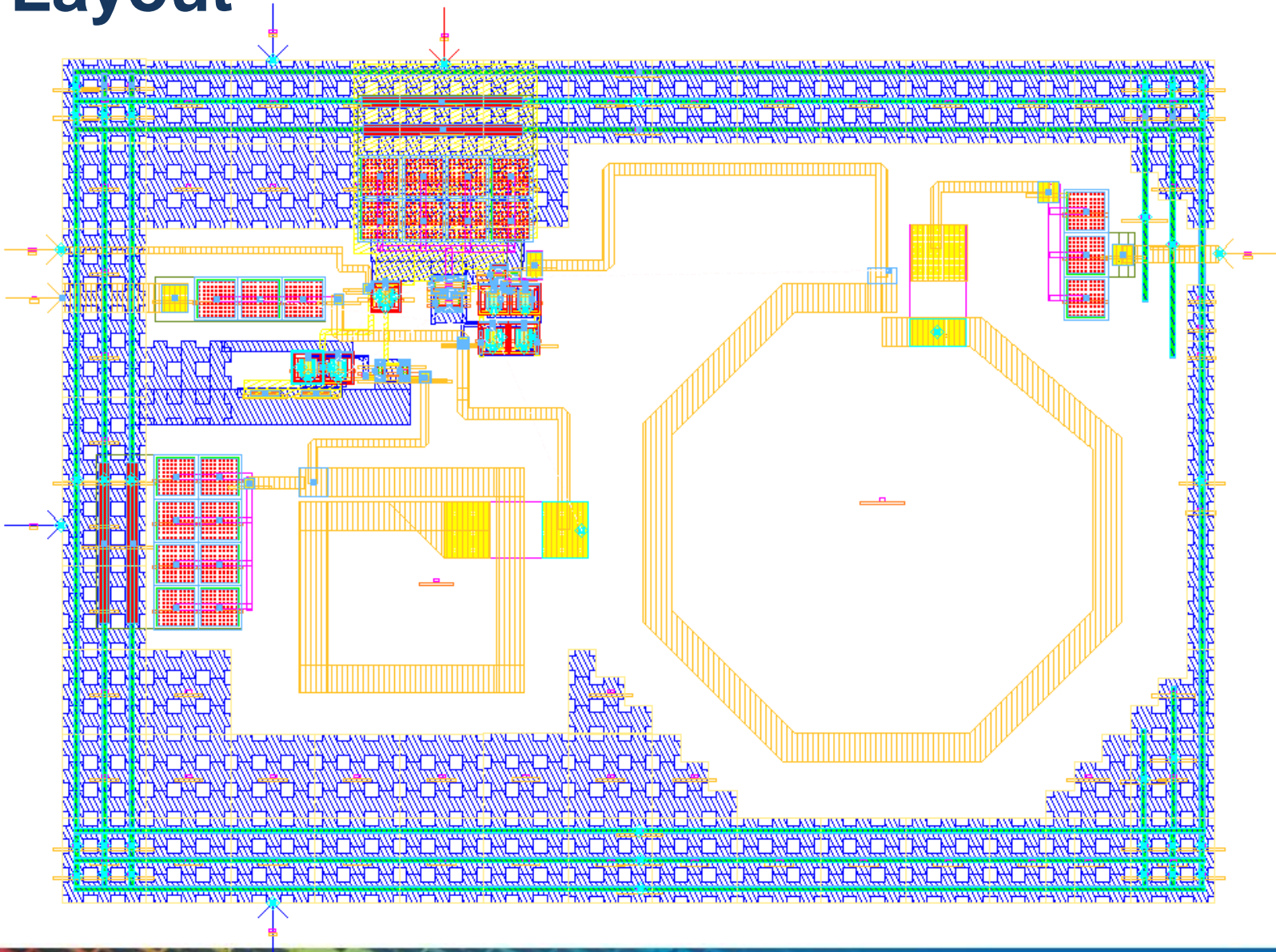
LNA with full PDK components – 2 tones



Observations

- Input and output are centered at 24GHz
- Maximum Gain at 18GHz
 - May be due to gm Slope ($f_0/f_t = 24/120 = 1/5$)
 - $20 \cdot \log 5 = 14\text{dB}$. Very close to limit.
 - To be proved

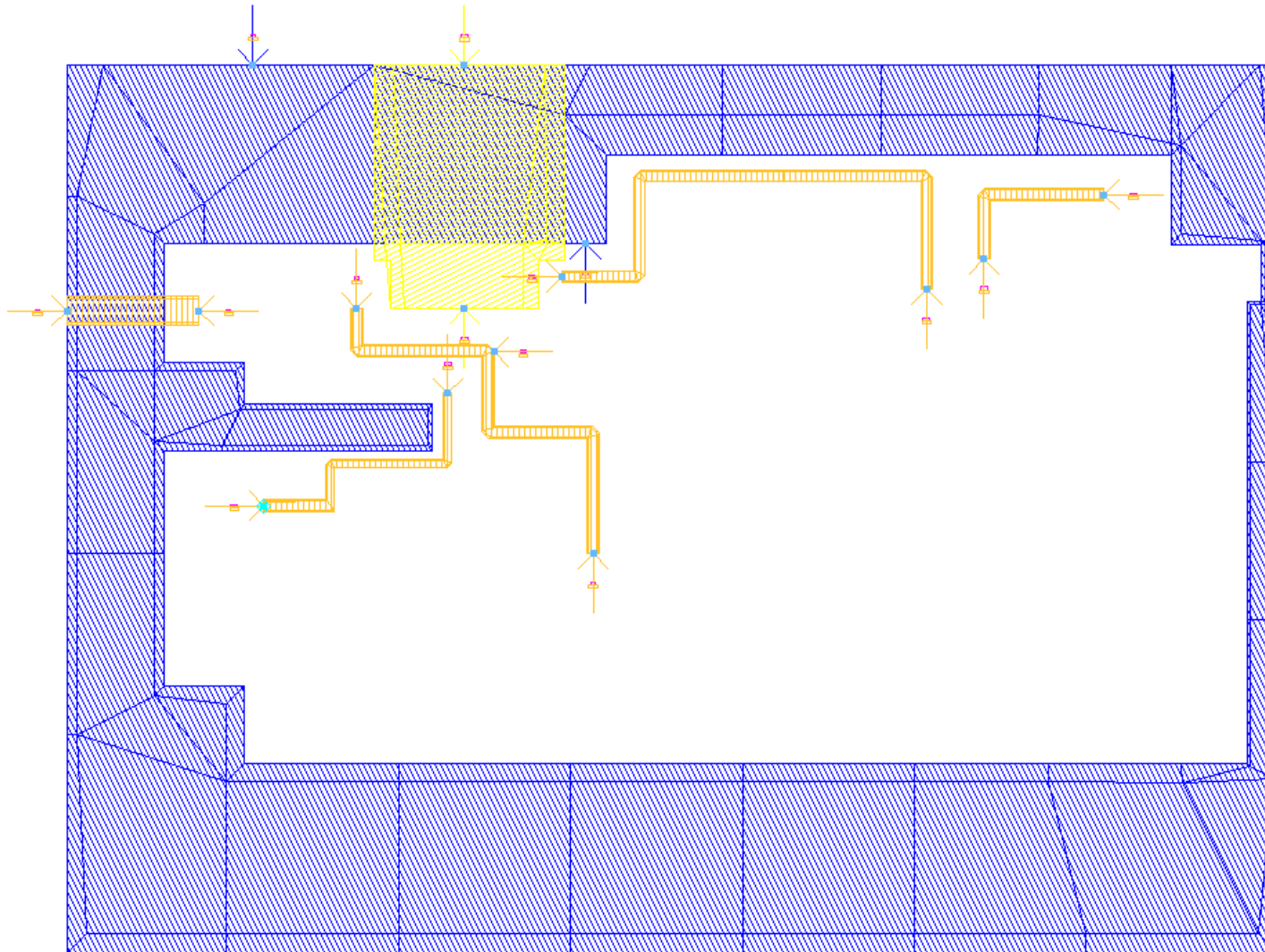
Layout



Layout Principles

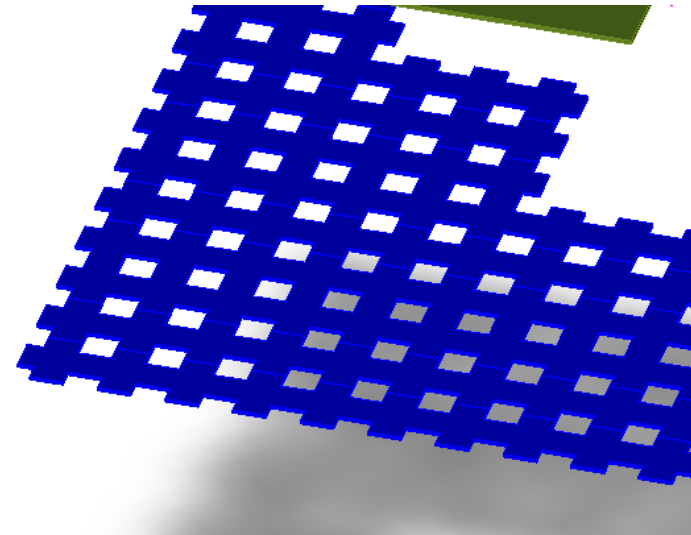
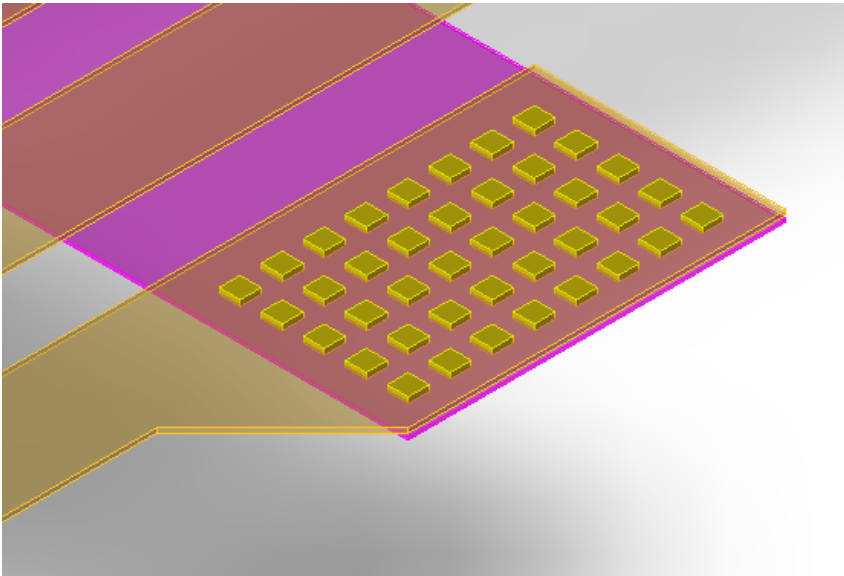
- **RF signals**
 - metal 6
 - Clearance area (minimum capacitance to GND)
 - As short as possible
- **Ground Plan**
 - Metal 1
 - Include a ring of contacts to GND
 - Better GND
 - Noise Isolation by bulk contacts
 - Ground plan is a “grid” like (metal density)
 - Assuming ground plan is part of larger plan
 - A ground plan / Supply plan Pcells are required
 - Ground in Metal 1
 - Supply in metal 2
- **Inductors**
 - Minimum 30 μ m clearance between inductors
 - Minimum 30 μ m clearance from Ground plan.
- **Ports**
 - Assuming close proximity of IN / OUT
 - If on of the above ports is distant – connect ports with 50 Ω transmission line
 - A transmission line Pcell is required

Layout for Momentum RF extraction

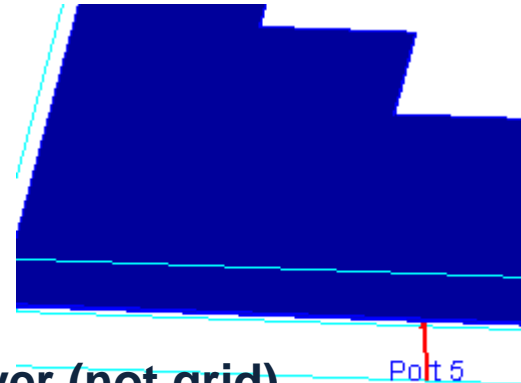


Layout for Momentum Principles

- Full layout is too big for Momentum
- Layout with mesh preview is presented



Layout for Momentum Principles



■ Simplification needed.

- Metal 1 Ground plan replaced by a solid layer (not grid)
- Metal 2 supply is simplifier
- Contacts to Ground caused failure of momentum calculations (non feasible results)
 - However, the bulk is defined as ground in Substrate file.
- 45° degrees edges caused a too complicated mesh.
- Limited frequency to 50GHz. Above - simulations became too heavy.
- Inductors where not added
 - Usually, RF extraction includes inductors for advanced parasitic extraction.
- Supply Ground
 - One port as source
 - Second post as circuit feed

Mesh Controls

Simulation Control

The image shows two overlapping software dialog boxes. The 'Mesh Setup Controls:46' dialog is in the foreground, and the 'Simulation Control:46' dialog is in the background.

Mesh Setup Controls:46

Global | Layer | Primitive | Primitive Seed

Define here the mesh values for the entire circuit

Preprocessor settings...

Mesh Frequency: 50 GHz

Mesh Density: 25 cells/wavelength

Arc Resolution (max. 45 deg): 45 degrees

Edge Mesh

Edge Width (leave empty or 0 for automatic size): 0 um

Transmission Line Mesh

Number of Cells Wide: 0

Thin layer overlap extraction

Mesh reduction

Horizontal side currents (thick conductors)

Buttons: OK, Reset, Clear, Cancel, Help

Simulation Control:46

Stimulus

Select a frequency plan from list to edit or define a new one

Type	F start	F stop	Npts/Step
Adaptive	0.0000 GHz	50.0000 GHz	50 max

Edit/Define Frequency Plan

Sweep Type: Adaptive

Start: 0 GHz

Stop: 50 GHz

Sample Points Limit: 50

Buttons: Paste, Update, Add to Frequency Plan List

Solution Files

Reuse files from the previous simulation

Dataset: Ina_3_F_4momentum_ra Browse...

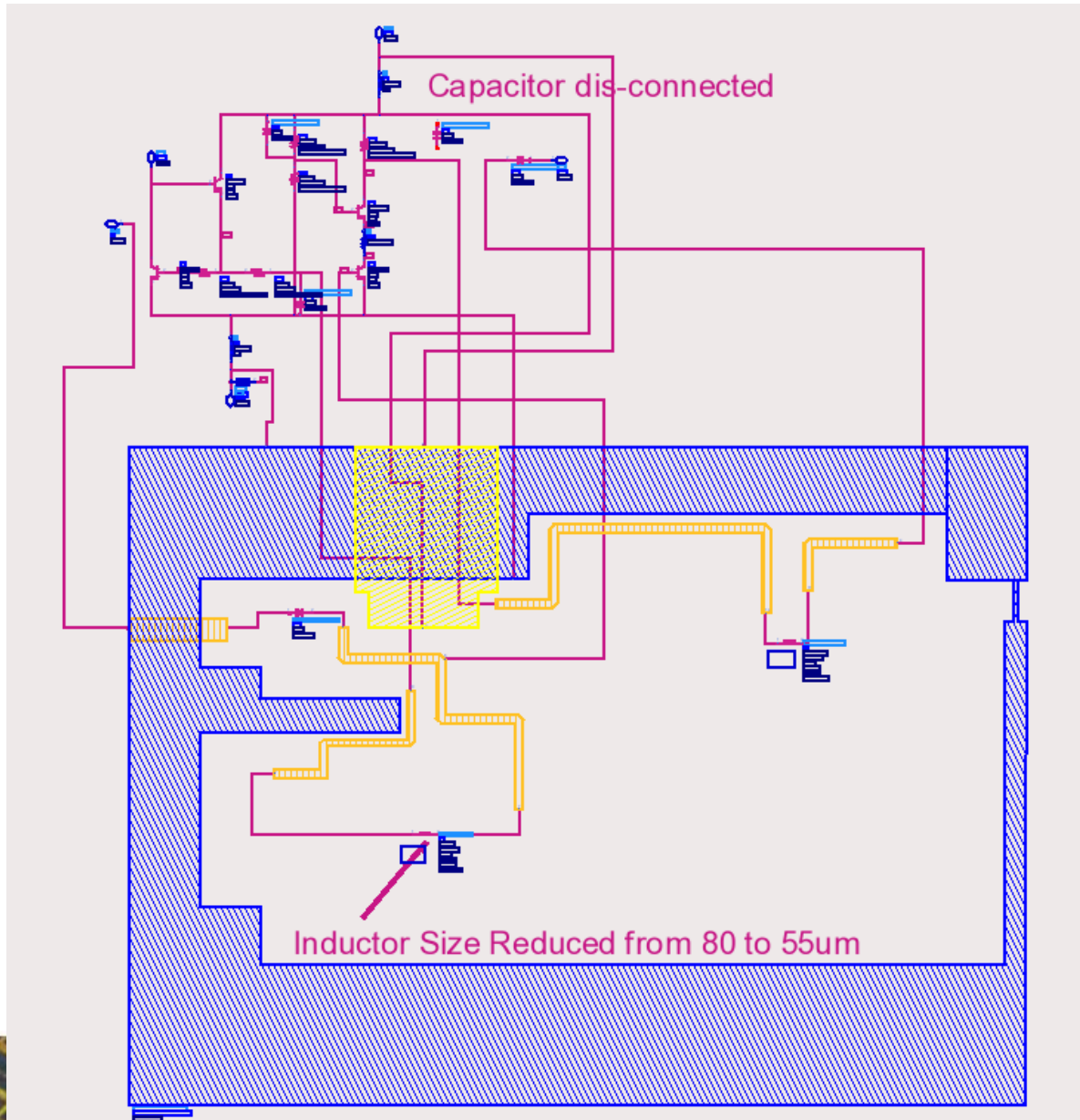
Data Display

Open data display when simulation completes

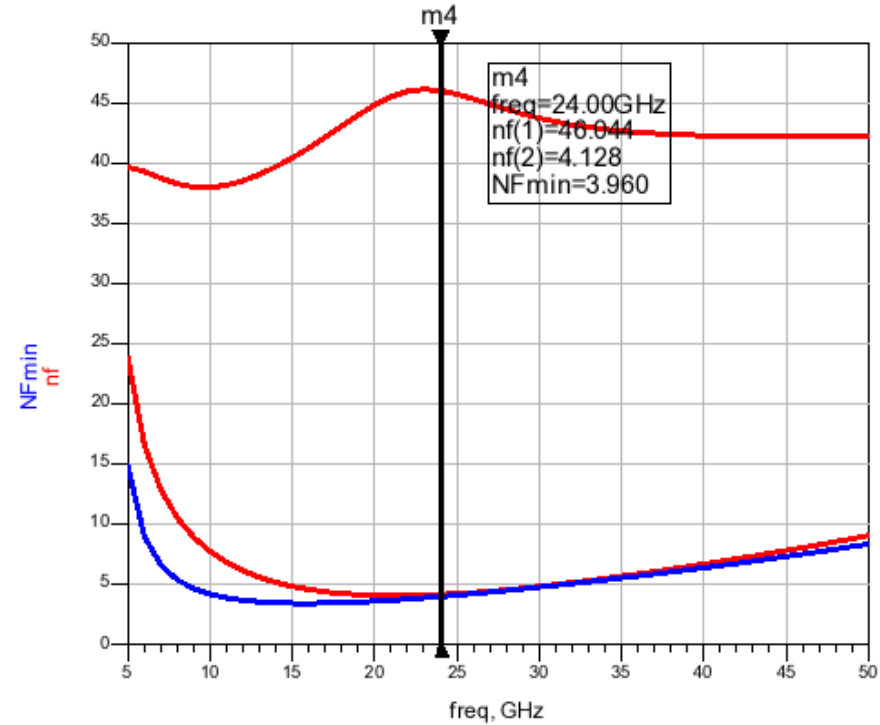
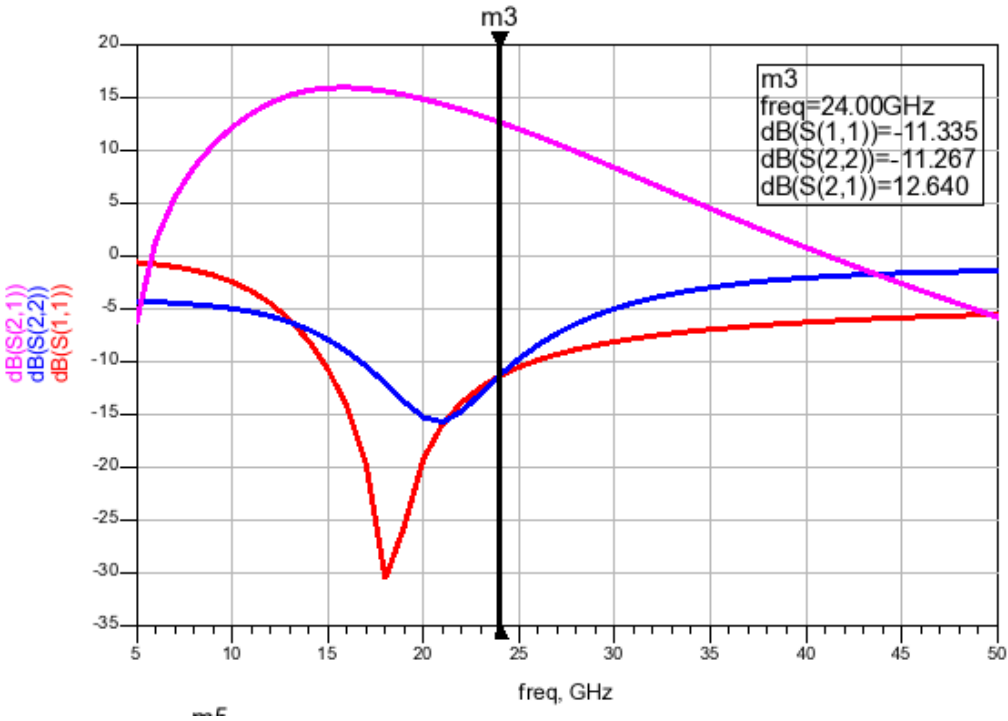
Template: Presentation1 Browse...

Buttons: Apply, Cancel, Help

Schematic and Momentum component



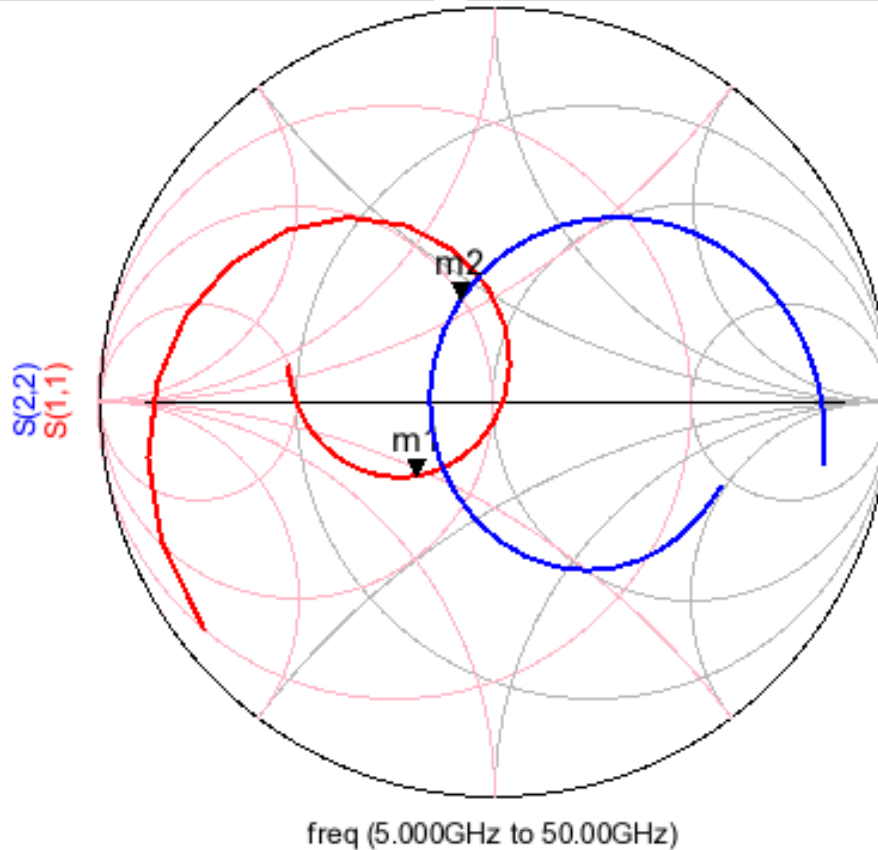
SP simulation with pre-layout components



Input Output impedance matching

m1
freq=24.00GHz
S(1,1)=0.271 / -136.399
impedance = $Z_0 * (0.632 - j0.255)$

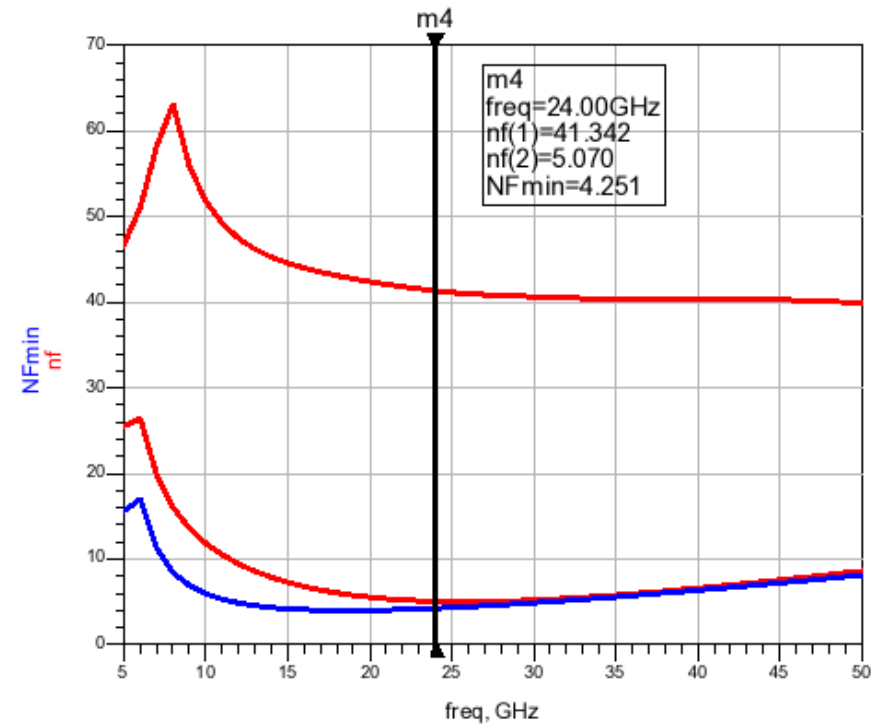
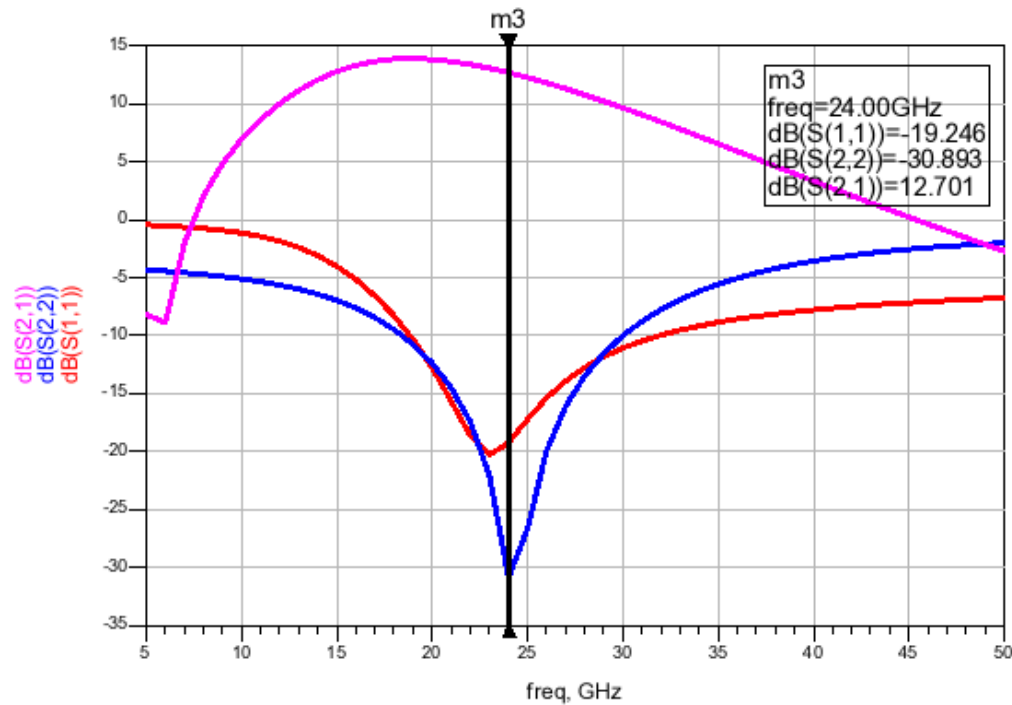
m2
freq=24.00GHz
S(2,2)=0.273 / 108.063
impedance = $Z_0 * (0.744 + j0.418)$



Adjusting components to re-tune LNA

- Load capacitor of 0.022 pF was totally removed
 - Wire capacitance is compensating.
- Input parallel inductor was reduced from 180pH to 140pH
 - Additional input capacitance to GND is resonated by a smaller inductor .

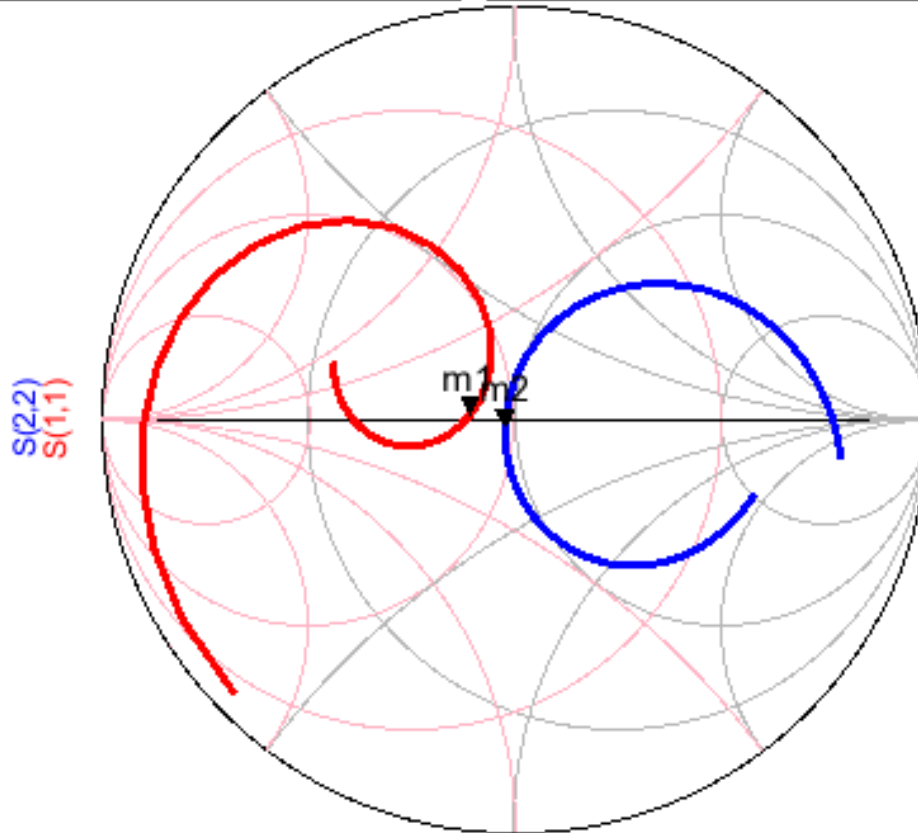
Post layout simulation after adjustment



Input Output impedance matching

m1
freq=24.00GHz
S(1,1)=0.109 / 174.469
impedance = $Z_0 * (0.804 + j0.017)$

m2
freq=24.00GHz
S(2,2)=0.029 / -146.151
impedance = $Z_0 * (0.953 - j0.030)$



freq (5.000GHz to 50.00GHz)

Observation

- **It is seen that input impedance is better Noise matched before corrections**
 - **Pre layout**
 - **NF = 5.118 dB**
 - **S21 = 12.92 dB**
 - **Post layout Before corrections**
 - **NF = 4.128 dB**
 - **S21 = 12.6dB**
 - **Post Layout After adjustment**
 - **NF = 5.07 dB**
 - **S21 = 12.7 dB**
- **However, this LNA was not matched for best NF**
- **Matching is for best S11, S22.**
- **Post Layout NF is better than pre-layout**

Summary

- Disclaimers:
 - No Package model
 - Partial optimization of OP
 - 24GHZ LNA with 5mA, NF = 5.1dB, Pgain = 12.7 dB
 - Input inductor final Q adds 0.3dB in NF
- TBDs
 - Lvs, Drc
 - Demonstration

TOWERjazz

www.towerjazz.com